	US ATLAS **HL-LHC Upgrade** **BASIS of ESTIMATE (BoE)**	**Date of Est:** 11/15/15 **Prepared by:** **A. Taffard, UCI** **Docdb #:**

WBS number:	**WBS Title: MDT Trigger firmware and advanced mezzanine card**
WBS Dictionary Definition:	
Estimate Type (check all that apply – see BOE Report for estimate type by activity): ___ Work Complete ___ Existing Purchase Order ___ Catalog Listing or Industrial Construction Database ___ Documented Vendor Estimate based on Drawings/ Sketches/ Specifications _X_ Engineering Estimate based on Similar Items or Procedures ___ Engineering Estimate based on Analysis _X_ Expert Opinion	
Supporting Documents (including but not limited to):	

Details of the Base Estimate (explanation of the Work)

The MDT trigger processor will employ ATCA carrier cards, each containing two advanced mezzanine cards (AMC). The MDT trigger processor uses a Xilinx Virtex 7 FPGA's as the main computational engine. A trigger processor FPGA will be installed on an AMC and perform the MDT trigger for a whole sector. Thus, a unit performs an octant (a small and a large sectors). A total of 32 units are necessary to cover the barrel and endcap. It expected that the same system could be used for the barrel and endcap, with possibly few firmware adjustments to deal with barrel/endcap specifics.

The hardware configuration is similar to the one used for the Phase-I New Small Wheel (NSW). The ATCA carrier cards are already being designed for Phase-I upgrade. It is expected that similar carrier cards would be designed (or adapted) for Phase-II.

This BoE covers the design, prototyping, production and testing of the AMC and of the firmware to be used to perform the segment finding and track fitting for an MDT trigger. The ATCA carrier cards and the firmware for the ancillary functions will be implemented elsewhere.

The core of the effort of the deliverable is in the design, production and testing of the AMC and the firmware.

There are three tasks described in this document. The first task comprises the design and testing of the firmware and the AMC with the construction of the first prototype follow by the identification and implementation of the changes for the pre-production prototype. The second task covers the pre-production prototype aimed to iterate on the design of the AMC and firmware and should exercise all the functionalities before committing to production mode. The final task takes place during the production phase and will encompass building the final hardware to be installed at CERN on the ATCA carrier card, and performing QA and QC. The schedule used for the estimate is based on the one presented in the ATLAS scoping document (LHCC-G-166). It is assumed that the hardware will need to be delivered at CERN mid-2024, for installation in USA15 early 2025.

6.x.2 MDT Trigger Hardware	Labor Hrs	Labor $	M&S $	Travel $	Total $
6.x.2.1 Firmware+AMC Design & Prototype	**11544**	**$1,019,879**	**$60,397**	**$26,170**	**$1,106,446**
Assoc Projc Sci	1776	$156,725			
Engineer	7104	$787,797			
Student	2664	$75,357			
M&S			$60,397		
Travel				$26,170	
6.x.2.2 Firmware+AMC Preproduction	**5772**	**$421,577**	**$46,939**	**$15,361**	**$483,877**
Engineer	2220	$258,080			
Technician	1332	$98,303			
Student	2220	$65,194			
M&S			$46,939		
Travel				$15,361	
6.x.2.3 Firmware+AMC Production & testing	**9324**	**$711,034**	**$424,777**	**$17,749**	**$1,153,560**
Engineer	3108	$378,199			
Technician	3108	$237,298			
Student	3108	$95,537			
M&S			$17,820.79		
Construction			$406,956.52		
Travel				$17,749	
MDT Trigger hardware	**26640**	**$ 2,152,489**	**$ 532,114**	**$ 59,280**	**$ 2,743,883**

Table 1: The deliverables from UC Irvine

During the first year, an Associate Project Scientist in collaboration with an Electrical Engineer will complete the development of the MDT trigger algorithm started during the R&D phase, and perform the optimization of the algorithm implementation onto the chosen hardware platform.
It is estimated that an Electrical Engineer (EE) and Electrical Engineer student are needed through the period of the project. An additional engineer will design the AMC during the design and prototype phase. The other EE will design the firmware for the trigger processor and develop necessary software for testing. The EE student will contribute to the testing and documentation of the test results. A Technician will be hired 9 months before the start of production to start developing the necessary software and test setup to perform QA and QC during the production phase. The technician will be in charge of the QA and QC. The salary rates were estimated based on the UCI rates in 2015. A 3% inflation rate was used to estimate the hourly rate during the construction years. The labor cost includes benefit.

The M&S contains the estimated cost of the prototypes (~$30k/ea.) and the cost of the cadence[1] and PCB design licenses ($4k and $1.5k respectively in 2015 and taking into account inflation).

Travel funding is included each year to support travel for the EE to CERN or domestic travel to from UCI to collaborative institutions such as UIUC or MU. Travel cost per year is based on two international trips of one-week from UCI to CERN for muon or TDAQ week and one domestic trip. Individual trip costs are based on past trips and include airfare, lodging and per-diem.

Overheard cost is accounted for labor, M&S and travel.

Assumptions:

We expect that the full specifications will be available on the timescale of the proposed work since a demonstrator based on commercial hardware will be developed during the former R&D phase.

Engineering will be available (hired at least one year before the start of the construction phase).
The primary physicist will be Anyes Taffard from UC-Irvine.

Risk Analysis

- Schedule Risk – Probability: *low*, Impact: *low*, Overall: *low*
    - Potential Problem: Currently, the project is at the conceptual design level. In particular specification of the AMC card as well as the final choice of FPGA. Communication between the trigger processor boards and the HEB and Sector Logic will also have to be defined, although it is expected that connection via GBT to HEB could be used. The details of the implementation of the firmware will be worked out during the R&D phase. However, similar trigger algorithms are currently being developed for the NSW which tighter time constraints. Initial studies for an MDT trigger have demonstrated the feasibility of the project.

[1] Cadence: Chip emulation and design software.

- Mitigation: Ensure that the specifications and choice of FPGA are defined by the end of the R&D phase. Ensure that there is a viable path for communication between boards and is accounted for in the latency calculation. It is expected that most of these will be defined during the R&D phase and experience gained with the NSW and implementation of the MDT trigger algorithm on emulation boards during the R&D phase will help in designing the algorithms. Experience gained in designing AMC cards for Phase-I or other Phase-II project will help mitigating risks.

- Cost Risk – Probability: *low*, Impact: *low*, Overall: *low*
  - Potential Problem: The cost estimate based on a conceptual design. The final choice of FPGA will affect the firmware implementation and the cost of the final hardware chosen for the production. Large amount of functionality packed into the firmware, resources available in the FPGA for fully functional firmware.
  - Mitigation: Studies will be made to find the best hardware solution. The algorithm will be designed in view of the hardware platform and optimized such to make the best usage of hardware capabilities while the most appropriate hardware will be chosen in view of the necessary tasks that need to be performed.

- Technical/Scope Risk – Probability: *low*, Impact: *low,* Overall: *low*
  - Potential Problem: ATCA crates are a fairly new system for ATLAS that will be used for the first time in Phase-I.
  - Mitigation: Work with other collaborators using ATCA carrier card and AMC to acquire knowledge in designing and operating working systems.

- External Risk – Probability: *low*, Impact: *low,* Overall: *low*
  - Potential Problem: The ATCA carrier cards will be developed elsewhere. Delay in delivery will reduce the testing time of the final MDT trigger processor system.
  - Mitigation: The schedule is flexible to accommodate modest delays. Work closely with other institutes to insure schedule is met.

Contingency Analysis

Will be done separately

Comments:

Quotes also go here

The cost estimate of the trigger electronics is based on conceptual designs only, which closely follow the design used for the NSW in Phase-I. Thus, this pertain a level of uncertainties.
At present, FPGA's and multicore architecture are rapidly evolving. With the recent purchase of Altera by Intel, one can expect FPGA performances to evolve in the coming years. Multicores look promising and optical fibers coming directly on the CPU chip offer an opportunity. Thus the final hardware choice on which the MDT trigger algorithm will be implemented may evolve from the one presented in this document. Since the hardware will be installed on AMC, this provides flexibility and permits to delay the choice of the hardware platform at a later stage of the R&D phase without increasing the risk to the project.

The Hit Extraction Boards (HEB) will deliver to the MDT trigger processor the MDT hits matching RPC/TGC RoIs and including the timing information for a whole sector. The MDT trigger processor will first perform the segment finding on each MDT layers and subsequently perform the track fitting to determine the muon momentum. The list of candidates, with their properties (eg, RoI, pT etc...) is then passed to the Sector Logic.

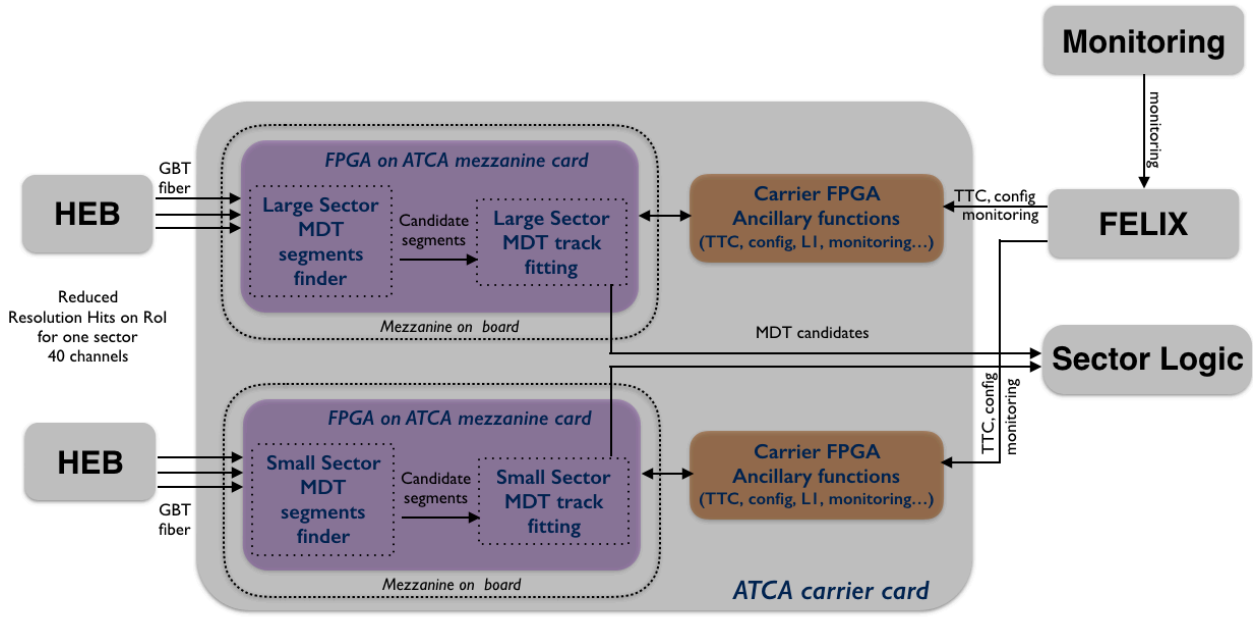

Figure 1: Conceptual design for the MDT trigger processor

Element TDAQ	Quantities	Unit Cost	Cost [CHF2015]
ATCA board base for MDT trigger processor			**16,500**
FPGA segment finding & track fitting	2	4,300	8,600
PCB	2	1,000	2,000
PCB assembly	2	300	600
PCB misc parts	2	250	500
ATCA carrier card	1	4,800	4,800

Element TDAQ	Quantities	Unit Cost	Cost [CHF2015]
Level-0 Muon Barrel			**478,280**
Barrel MDT Trigger	**1**		**441,280**
Trigger Board (ATCA)	16	16,500	264,000
Fiber to HEB (12 lanes fibers) ????	96	1,800	172,800
Fiber to SL - assume 7 duplicates sent to SL	224	20	4,480
ATCA crates	**2**	**18,500**	**37,000**
Crate -- 14 slots	1	13,000	13,000
Switch	1	4,000	4,000
PSU	0	4,000	-
Server	0.5	3,000	1,500

Element TDAQ	Quantities	Unit Cost	Cost [CHF2015]
Level-0 Muon Endcap			**478,280**
Endcap MDT Trigger	**1**		**441,280**
Trigger Board (ATCA)	16	16,500	264,000
Fiber to HEB (12 lanes fibers) ????	96	1,800	172,800
Fiber to SL - assume 7 duplicates sent to SL	224	20	4,480
ATCA crates	**2**	**18,500**	**37,000**
Crate -- 14 slots	1	13,000	13,000
Switch	1	4,000	4,000
PSU	0	4,000	-
Server	0.5	3,000	1,500

Table 2: Cost estimate for the whole MDT trigger processor system

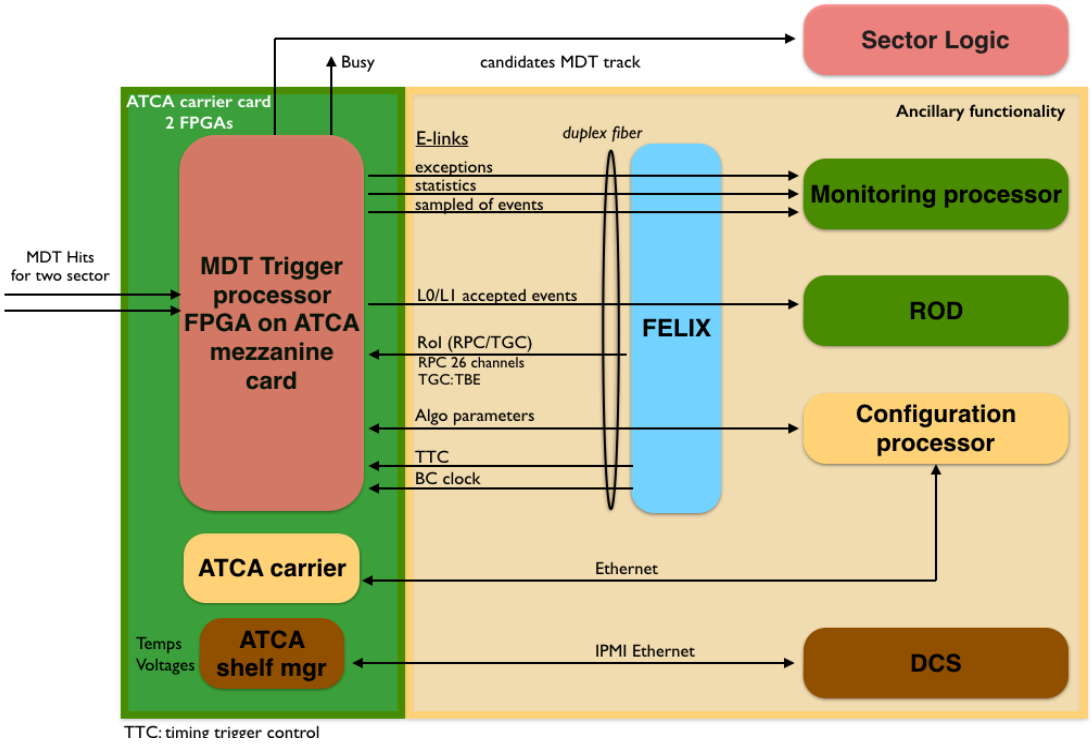

Figure 2: Context diagram for an MDT trigger processor board